CLAIMS

1. (Currently amended) A frequency synthesizer for generating a data-modulated output signal based on a reference signal and an input data signal, the frequency synthesizer comprising:

(a) a phase-locked loop (PLL) circuit configured to receive the reference signal and generate the data-modulated output signal;

(b) a first data-modulation path configured to (i) generate a first data-modulated input signal based on the input data signal and (ii) apply the first data-modulated input signal at a voltage-controlled oscillator (VCO) of the PLL circuit; and

(c) a second data-modulation path configured to (i) generate a second data-modulated input signal based on the input data signal and (ii) ~~apply~~ provide the second data-modulated input signal at a frequency divider of the PLL circuit to control the divider's division factor.

2. (Original) The invention of claim 1, wherein the first and second data-modulated input signals have substantially complementary frequency responses.

3. (Original) The invention of claim 1, wherein:

the PLL circuit comprises a phase detector, a loop filter connected to the phase detector, the VCO connected to the loop filter, and the frequency divider, which is part of a feedback path connecting the VCO and the phase detector.

4. (Original) The invention of claim 3, wherein:

the first data-modulation path has a high-pass frequency response corresponding substantially to a corner frequency of the loop filter; and

the second data-modulation path has a low-pass frequency response corresponding substantially to the corner frequency of the loop filter.

5. (Original) The invention of claim 3, wherein:

the phase detector is configured to generate a phase-difference signal based on the reference signal and a frequency-divided signal from the frequency divider;

the loop filter is configured to generate a loop-filtered signal based on the frequency-divided signal from the phase detector;

the VCO is configured to generate the data-modulated output signal based on the loop-filtered signal from the loop filter and the first data-modulated input signal from the first data modulation path; and

the frequency divider is configured to generate the frequency-divided signal based on the data-modulated output signal from the VCO and the second data-modulated input signal from the second data modulation path, wherein the second data-modulated input signal determines a division factor applied by the frequency divider to the data-modulated output signal to generate the frequency-divided signal.

6. (Original) The invention of claim 1, wherein the second data modulation path comprises a sigma-delta modulator configured to generate the second data-modulated input signal based on the input data signal.

7. (Original) The invention of claim 6, wherein frequency synthesizer is configured to operate with two or more different reference signals and the second data modulation path further comprises:

a scaling block configured to adjust gain of the second data modulation path based on a selected reference signal; and

a carrier-selection block configured to inject a carrier frequency based on the selected reference signal.

8. (Original) The invention of claim 6, wherein the frequency synthesizer applies Gaussian frequency shift keying (GFSK) data modulation and the input data signal is Gaussian low-pass filtered prior to application to the first and second data modulation paths.

9. (Original) The invention of claim 6, wherein the sigma-delta modulator quantizes spurious signals to high frequencies that are attenuated within the PLL circuit.

10. (Original) The invention of claim 6, wherein the sigma-delta modulator comprises:
(i) an adder; and
(ii) a noise-shaping loop, wherein:
the adder is configured to generate a summation signal based on the input data signal and an output signal from the noise-shaping loop, wherein:
a set of one or more most significant bits (MSBs) of the summation signal corresponds to the second data-modulation input signal applied to the frequency divider; and
a set of one or more least significant bits (LSBs) of the summation signal is fed back as an input signal to the noise-shaping loop.

11. (Original) The invention of claim 10, wherein the sigma-delta modulator functions as a quantizer with quantization error fed back into the quantizer via the noise-shaping loop.

12. (Original) The invention of claim 1, wherein the VCO is an analog VCO, the first data-modulated input signal is an analog signal, and the first data modulation path comprises a digital-to-analog converter (DAC) to generate the analog first data-modulated input signal.

13. (New) A frequency synthesizer for generating a data-modulated output signal based on a reference signal and an input data signal, the frequency synthesizer comprising:
(a) a phase-locked loop (PLL) circuit configured to receive the reference signal and generate the data-modulated output signal;
(b) a first data-modulation path configured to (i) generate a first data-modulated input signal based on the input data signal and (ii) apply the first data-modulated input signal at a voltage-controlled oscillator (VCO) of the PLL circuit; and
(c) a second data-modulation path configured to (i) generate a second data-modulated input signal based on the input data signal and (ii) apply the second data-modulated input signal at a frequency divider of the PLL circuit, wherein the first and second data-modulated input signals have substantially complementary frequency responses.

14. (New) A frequency synthesizer for generating a data-modulated output signal based on a reference signal and an input data signal, the frequency synthesizer comprising:
(a) a phase-locked loop (PLL) circuit configured to receive the reference signal and generate the data-modulated output signal, wherein the PLL circuit comprises a phase detector, a loop filter connected to the phase detector, the VCO connected to the loop filter, and the frequency divider, which is part of a feedback path connecting the VCO and the phase detector;
(b) a first data-modulation path configured to (i) generate a first data-modulated input signal based on the input data signal and (ii) apply the first data-modulated input signal at a voltage-controlled oscillator (VCO) of the PLL circuit; and

(c) a second data-modulation path configured to (i) generate a second data-modulated input signal based on the input data signal and (ii) apply the second data-modulated input signal at a frequency divider of the PLL circuit, wherein:

the first data-modulation path has a high-pass frequency response corresponding substantially to a corner frequency of the loop filter; and

the second data-modulation path has a low-pass frequency response corresponding substantially to the corner frequency of the loop filter.

15. (New) A frequency synthesizer for generating a data-modulated output signal based on a reference signal and an input data signal, the frequency synthesizer comprising:

(a) a phase-locked loop (PLL) circuit configured to receive the reference signal and generate the data-modulated output signal;

(b) a first data-modulation path configured to (i) generate a first data-modulated input signal based on the input data signal and (ii) apply the first data-modulated input signal at a voltage-controlled oscillator (VCO) of the PLL circuit; and

(c) a second data-modulation path configured to (i) generate a second data-modulated input signal based on the input data signal and (ii) apply the second data-modulated input signal at a frequency divider of the PLL circuit, wherein:

the second data modulation path comprises a sigma-delta modulator configured to generate the second data-modulated input signal based on the input data signal, wherein the sigma-delta modulator comprises:

(i) an adder; and

(ii) a noise-shaping loop, wherein the adder is configured to generate a summation signal based on the input data signal and an output signal from the noise-shaping loop, wherein:

a set of one or more most significant bits (MSBs) of the summation signal corresponds to the second data-modulation input signal applied to the frequency divider; and

a set of one or more least significant bits (LSBs) of the summation signal is fed back as an input signal to the noise-shaping loop.

16. (New) The invention of claim 15, wherein the sigma-delta modulator functions as a quantizer with quantization error fed back into the quantizer via the noise-shaping loop.